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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,403	03/30/2004	Yasumasa Tsukamoto	67161-149	1709

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MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/812,403	TSUKAMOTO, ET AL.
	Examiner	Art Unit
	Gene N. Auduong	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3-30-04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on March 30, 2004 is being considered by the examiner.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Itoh et al. (U.S. Pat. No. 6,046,627).

Regarding claim 1, Itoh et al. disclose a semiconductor memory device as in figure 3, comprising: a plurality of memory cells (array of SRAM cells), arranged in rows and columns, each including a latch circuit formed of insulated gate type field effect transistors of first and second conductivity types each having a back gate (SRAM cells array, col. 5, lines 40+); and substrate potential changing circuitry (substrate voltage generating and controlling circuit) for

changing a back gate potential of at least the insulated gate type field effect transistor of the first conductivity type of a selected memory cell in a data writing from the back gate potential in a data reading in response to an address signal and an operation mode designating signal (col. 5, lines 51+; col. 8, lines 65+).

Regarding claims 2-4 and 7-9, Itoh et al. disclose the semiconductor memory device according to claim 1, wherein the insulated gate type field effect transistor of the first conductivity type is a P/N channel insulated gate type field effect transistor, and the substrate potential changing circuitry sets the back gate potential of the P/N channel insulated gate type field effect transistor of the selected memory cell in the data writing to a voltage level higher/lower than in the data reading; wherein the substrate potential changing circuitry sets the back gate potential of the P/N channel insulated gate type field effect transistor to an external interfacing power supply/ground voltage level in the data writing; and/or wherein each of the memory cells receives a power source/ground voltage as a power supply voltage for high/low level data storage, and the substrate potential changing circuitry sets the back gate potential of the P/N channel insulated gate type field effect transistor to the power source/ground voltage level in the data writing and to a voltage level lower/higher than the power source/ground voltage in the data reading (figure 1 and 3; col. 5, lines 51+; col. 8, lines 65+).

Regarding claims 5, 10 and 12, Itoh et al. disclose the semiconductor memory device according to claim 1, wherein the substrate potential changing circuitry includes a plurality of substrate voltage transmission lines, arranged corresponding to the respective memory cell columns, each coupled commonly to the back gates of the insulated gate type field effect transistors of the first conductivity type in a corresponding column, and a plurality of substrate

potential setting circuits, arranged corresponding to the respective columns, each for setting a voltage of a corresponding substrate voltage transmission line in response to the operation mode designating signal and a column select signal generated based on the address signal (figures 1;3 and other related figures).

Regarding claims 6 and 11, Itoh et al. disclose the semiconductor memory device according to claim 5, wherein the insulated gate type field effect transistor of the first conductivity type is a P channel insulated gate type field effect transistor, and the substrate potential changing circuitry makes a back gate potential of the P channel insulated gate type field effect transistor in a selected column higher than in the memory cell on a non-selected column when the operation mode designating signal designates the data writing (figure 1 and 3; col. 5, lines 51+; col. 8, lines 65+).

Regarding claim 13, Itoh et al. disclose the semiconductor memory device according to claim 1, wherein the insulated gate type field effect transistor of the first conductivity type of the memory cell is formed in a first substrate region, and the insulated gate type field effect transistor of the second conductivity type of the memory cell is formed in a second substrate region, the first and second substrate regions are each formed, continuously in a column direction, corresponding to each column, and form the back gates of the insulated gate type field effect transistors of the first and second conductivity type, respectively, of the memory cells arranged in a corresponding column, and the substrate potential changing circuitry changes a potential of at least one of the first and second substrate regions (figures 4 and 8).

Regarding claim 14, Itoh et al. disclose the semiconductor memory device according to claim 13, further comprising a power line extending continuously in a column direction and

commonly coupled to the insulated gate type field effect transistors of the first conductivity type of the memory cells arranged in alignment in the column direction (figures 1, 3 and 10).

Regarding claim 15, Itoh et al. disclose the semiconductor memory device according to claim 13, wherein the first and second substrate regions are formed on an insulating film, and the first and second substrate regions are isolated by a trench region (figures 4 and 8).

Regarding claim 16, Itoh et al. disclose the semiconductor memory device according to claim 15, wherein the first and second substrate regions are isolated in units of columns (figures 8 and 13-14).

Regarding claim 17, Itoh et al. disclose the semiconductor memory device according to claim 1, wherein the substrate potential changing circuitry changes a potential application manner of the back gates for the plurality of memory cells between a standby state, the data reading and the data writing, in response to the operation mode designating signal (col. 5, lines 51+; col. 8, lines 65+).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
August 30, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827